

6/2002

Classroom - Mac 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

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- US-to-IPC Concordances
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499 **INTEGRATED CIRCUIT STRUCTURE WITH**  
**ELECTRICALLY ISOLATED COMPONENTS**  
 500 . Including high voltage or high power devices isolated from low voltage or low power devices in the same integrated circuit  
 501 .. Including dielectric isolation means  
 502 .. High power or high voltage device extends completely through semiconductor substrate (e.g., backside collector contact)  
 503 . With contact or metallization configuration to reduce parasitic coupling (e.g., separate ground pads for different parts of integrated circuit)  
 504 . Including means for establishing a depletion region throughout a semiconductor layer for isolating devices in different portions of the layer (e.g., "JFET" isolation)  
 505 . With polycrystalline semiconductor isolation region in direct contact with single crystal active semiconductor material  
 506 . Including dielectric isolation means  
 507 .. With single crystal insulating substrate (e.g., sapphire)  
 508 .. With metallic conductor within isolating dielectric or between semiconductor and isolating dielectric (e.g., metal shield layer or internal connection layer)  
 509 .. Combined with pn junction isolation (e.g., isoplanar, LOCOS)  
 510 ... Dielectric in groove  
 511 .... With complementary (npn and pnp) bipolar transistor structures)  
 512 .... Complementary devices share common active region (e.g., integrated injection logic, I<sup>2</sup>L)  
 513 .... Vertical walled groove  
 514 .... With active junction abutting groove (e.g., "walled emitter")  
 515 .... With active junction abutting groove (e.g., "walled emitter")  
 516 .... With passive component (e.g., resistor, capacitor, etc.)  
 517 .... With bipolar transistor structure  
 518 .... With polycrystalline connecting region (e.g., polysilicon base contact)  
 519 .... Including heavily doped channel stop region adjacent groove  
 520 .... Conductive filling in dielectric-lined groove (e.g., polysilicon backfill)  
 521 .... Sides of grooves along major crystal planes (e.g., (111), (100) planes, etc.)  
 522 .. Air isolation (e.g., beam lead supported semiconductor islands)

Document Title  
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U	I	Document ID	Issue Date	Pages	Title	Current OR	Retrieval C	Inventor	S	C	P	Y	3	US
1		US 6402931 B1	20020611	18	Electrochemical machining using modulated reverse	205/659		Zhou, Chengdong et al.						US
2		US 6319384 B1	20011120		Pulse reverse electrodeposition for	205/103		Taylor, E. Jennings et al.						
3		US 6309528 B1	20011030		Sequential electrodeposition of metals using modulated	205/103		Taylor, E. Jennings et al.						
4		US 6303014 B1	20011016		Electrodeposition of metals in small recesses using	205/103		Taylor, E. Jennings et al.						
5		US 6210555 B1	20010403		Electrodeposition of metals in small recesses for	205/103		Taylor, E. Jennings et al.						
6		US 6203684 B1	20010320		Pulse reverse electrodeposition for	205/103		Taylor, E. Jennings et al.						
7		US 6080504 A	20000627		Electrodeposition of catalytic metals using	429/42		Taylor, E. Jennings et al.						
8		US 5804057 A	19980908		Method of removing metal salts from solution by	205/702		Zhou, Chengdong et al.						
9		US 5695622 A	19971209		Electrode for peroxide generator and method for	204/292		Fraser, Mark E. et al.						
10		US 5647968 A	19970715		Process for making peroxide	205/466		Fraser, Mark E. et al.						
11		US 5599437 A	19970204		Electrolysis of electroactive species using	205/744		Taylor, E. Jennings et al.						
12		US 5565073 A	19961015		Electrochemical peroxide generator	204/256		Fraser, Mark E. et al.						





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DOCUMENT-IDENTIFIER: US 6402931 B1  
TITLE: Electrochemical machining using modulated reverse electric fields

----- RWIC -----

IN22:

Taylor: E. Nunnally

US 6,402,931 B1

15

12 provide a total anodic on-time of 20 seconds. The voltage during the forward (anodic) pulse was 20 volts, while the voltage during the reverse (cathodic) pulse was three volts. The parameters of the experiments are set forth in Table 3 below.

TABLE 3

Test No.	Area (cm <sup>2</sup> )	Time (min)	Off time (min)	On time (min)	Temp (°C)	Flow rate (cc/min)	On time (min)
1	DC	10	10	10	100	1.8	51-63
2	PC	10	10	10	100	1.8	61-71
3	MRC	10	10	10	100	1.8	69-72
4	PC	40	20	20	100	1.8	61-71
5	PC	40	20	20	100	1.8	69-72
6	MRC	40	20	20	100	1.8	69-72
7	MRC	40	20	20	100	1.8	69-72
8	MRC	40	20	20	100	1.8	69-72

After each experiment the thickness of material removed was determined by measuring the depth of the depression in the surface of the coupon produced by the experiment. The surface of the electropolished area of the workpiece 402 was visually evaluated for smoothness and smoothness. The surface roughness was quantitatively evaluated with a profilometer (SURFTEST SV502). The surface roughness measured by the profilometer is expressed as an Ra value, defined as the arithmetic mean of the absolute value of the distance from the mean line to the profile. The results of the experiments are set forth in Table 4 below and in FIGS. 12A, 12B, 13A, 13B, 14A, and 14B, which are photomicrographs showing the surfaces produced by certain of the experiments. Based on the flow pattern of the electrolyte, the electrochemically polished surface was divided into two regions for surface quality evaluation, as indicated in FIG. 11. The central area of the test surface where the electrolyte flow impinges directly on the workpiece surface 410 is identified in Table 4 and FIG. 11 as the P-area 418. The annular area surrounding the P-area 418, where the electrolyte flow is generally parallel to the workpiece surface 410, is identified in Table 4 and FIG. 11 as the S-area 420.

TABLE 4

Test No.	Type	Area (cm <sup>2</sup> )	P-area (cm <sup>2</sup> )	S-area (cm <sup>2</sup> )	Surface roughness (Ra)	Depth of material removed (mm)	Micro-etching	
							Surface quality (mm)	Depth of material removed (mm)
1	DC	10	10	10	0.51	100-150	100-150	100-150
2	PC	10	10	10	0.57	100-150	100-150	100-150
3	MRC	10	10	10	0.47	100-150	100-150	100-150
4	PC	40	20	20	0.38	50-100	50-100	50-100
5	PC	40	20	20	0.23	50-100	50-100	50-100
6	MRC	40	20	20	0.23	50-100	50-100	50-100
7	MRC	40	20	20	0.23	50-100	50-100	50-100
8	MRC	40	20	20	0.23	50-100	50-100	50-100

--- = shiny and smooth

--- = semi-shiny and smooth

The data establish that the surface formed by electropolishing using MRC is generally superior to that formed by either DC or PC electrochemical polishing. It is notable that

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the surface roughness for PC is generally greater than for DC, i.e., the surface quality is inferior. On the other hand MRC produces a surface that is smoother than either DC or PC electrochemical polishing. The superior quality of the surface achieved with MRC electrochemical polishing is also seen in the fewer number of defects and the general visual appearance of the surface, which appears smooth and shiny. The appearance of the surface prepared by DC, PC and MRC can also be compared by referring to FIGS. 12A, 12B, 13A, 13B, 14A and 14B. FIGS. 12A and 12B are micrographs at 200x of the P-area and S-area, respectively, of the surface achieved using PC. FIGS. 14A and 14B are micrographs at 200x of the P-area and S-area, respectively, of the surface achieved using MRC. A comparison of the micrographs readily reveals that the smoothest surface is achieved by using modulated reverse current (MRC).

The invention having now been fully described, it should be understood that it may be embodied in other specific forms or variations without departing from its spirit or essential characteristics. Accordingly, the embodiments described above are to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

We claim:

1. A method for electrochemical deburring of a metal substrate comprising:
  - a) interposing an electrolyte between a metallic substrate including burrs and an electrically conductive tool, and passing an electric current between said tool and said substrate to effect anodic dissolution of said burrs, wherein said electric current is a pulsed current comprised of anodic pulses and cathodic pulses wherein said cathodic pulses are interposed between at least some of said anodic pulses, said anodic pulses have a pulse width of from about 1 ms to about 50 ms and said anodic pulses have a frequency between about 5 Hertz and about 500 Hertz.
  2. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses.
  3. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses.
  4. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses and between said cathodic pulses and succeeding anodic pulses.
  5. The method of claim 1 wherein said cathodic pulses and said anodic pulses succeed each other without intervening intervals of no electric current flow.
  6. The method of claim 1 wherein said anodic pulses have a frequency between about 10 Hertz and about 300 Hertz.
  7. The method of claim 1 wherein said anodic pulses have a frequency between about 10 Hertz and about 100 Hertz.
  8. The method of claim 1 wherein said anodic pulses have a pulse width of from about 1 ms to about 50 ms.



Document ID	Pages	1	2	3	4	5	6	7	8	9	10	11	12	Kind	Codes	Source
US 6402931 B1	18															USPAT
US 6319384 B1	12															USPAT
US 6309528 B1	12															USPAT
US 6303014 B1	24															USPAT
US 6210555 B1	14															USPAT
US 6203684 B1	11															USPAT
US 6080504 A	10															USPAT

DOCUMENT-IDENTIFIER: US 6319384 B1  
TITLE: Pulse reverse electrodeposition for metallization and planarization of semiconductor substrates

----- RWTC -----

IN22:  
Taylor, B. Jennings

# US 6,319,384 B1

11

damascene-prepared surface wherein the thickness of the metal layer deposited on the surface portions of semiconductor wafers metallized by the process of the invention will be no greater than the depth of metal deposited in the trenches. Preferably, the thickness of the surface layer will be substantially less than the depth of metal deposited in the trenches, e.g., no greater than about 80% of the depth of metal deposited in the trenches. More preferably, the thickness of the surface metal layer will amount to only about 50%, or even 10% or less of the depth of metal deposited in the trenches.

The process of the invention can also be applied to deposition of a uniform metal layer on the surface of a semiconductor wafer, as is required for some manufacturing procedures. The application of the process of the invention to such wafers is illustrated in FIGS. 4A-4D.

FIG. 4A illustrates schematically a cross-section of a semiconductor wafer that has been cut from a single crystal of a semiconductor, e.g., silicon. Such wafers are typically round and very thin. In order to metallize the surface of the wafer, a barrier layer (not shown) and a very thin conducting layer (not shown) are deposited, e.g., by CVD, as for the case of the damascene-prepared surface discussed above.

When a metal is deposited on the surface of such a wafer, the non-uniform distribution of current at the edges of the wafer gives rise to excess metal deposition at the edge. The excess metal causes the surface of the plated wafer to be somewhat nonplanar, and can interfere with subsequent manufacturing operations unless it is removed or prevented.

In order to avoid the problem of excess metal deposition at the edge of the wafer 400 without resorting to the use of auxiliary electrodes ("robbers"), shields positioned in the electroplating bath, or the like, the plating can be conducted using modulated reverse electric fields according to the invention.

FIG. 4B shows an enlarged cross section of the edge of the wafer 400 as indicated by the circle 4B in FIG. 4A. A metal layer 406 is shown schematically and with exaggerated thickness as deposited on the surface 404 of the wafer 400 near its edge 404 after the first, relatively short, cathodic current pulse. As discussed above for the damascene-prepared surface, because the cathodic pulse is of finite duration, there may be some non-uniformity in the deposition of the metal layer, as shown by the excess metal 408 deposited at the edge 404 of the wafer 400.

FIG. 4C shows schematically the configuration of the deposited metal layer after a subsequent anodic pulse of relatively long duration. Such a long anodic pulse will remove metal non-uniformly and preferentially from the elevated and/or convex portions of the wafer surface. Accordingly, the excess metal 408 that may have been deposited by the cathodic pulse tends to be removed by a subsequent anodic pulse.

FIG. 4D shows schematically the plated metal layer 406 at the edge 404 of the wafer 400 after the plating has been completed. The plated layer 406 ideally extends smoothly and with essentially constant thickness to the edge of the wafer. Furthermore, the plated metal layer 406 will also tend to fill any microscopic depressions in the surface 404 of the wafer 400.

The method of the invention may be used with any metal that can be deposited by electroplating techniques. Thus copper, silver, gold, zinc, chromium, nickel, and alloys thereof such as bronze, brass, and the like, may be applied to microcircuit surfaces by the process of the invention. The invention is particularly useful in filling trenches and vias in

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damascene-prepared surfaces generated in the manufacture of VLSI semiconductor devices and the like and in preparing planar layers of metal on large-diameter semiconductor wafers.

The electroplating bath used in the process of the invention can be any conventional electroplating bath appropriate for the metal being plated. For electroplating copper onto a semiconductor surface, particularly when preparing microcircuit conductors by the damascene process, it is preferred to avoid conventional additives such as leveling agents and the like to the extent possible in order to avoid the difficulties of using such additives such as possible inclusion in the plated conductors. A preferred bath for electroplating copper onto a semiconductor surface is an aqueous acidic copper sulfate bath incorporating about 40 to about 80 g/L of copper sulfate, a molar ratio of sulfuric acid to copper sulfate of about 5:1 to about 8:1, about 5% of polyethylene glycol and about 30 ppm to about 60 ppm of chloride ions. A pulse train frequency of about 1000 Hz with a cathodic duty cycle of about 20%, an anodic duty cycle of about 75% and a cathodic/anodic charge transfer ratio of 5 or less appeared to give superior results.

The invention having now been fully described, it should be understood that it may be embodied in other specific forms or variations without departing from its spirit or essential characteristics. Accordingly, the embodiments described above are to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

We claim:

1. A method for depositing a smooth layer of a metal on a microcircuit substrate comprising:  
immersing an electrically conductive substrate having a microcircuit surface in an electroplating bath containing ions of a metal to be deposited onto said surface, said plating bath being substantially devoid of leveling, immersing a counter electrode in said plating bath passing an electric current between said substrate and said counter electrode,

wherein

said electric current is a modulated reversing electric current comprising a train of pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate,

said cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%.

the charge transfer ratio of said cathodic pulses to said anodic pulses is greater than one, and the frequency of said train of pulses ranges from about 10 Hertz to about 13000 Hertz.

2. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses.

3. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses.

4. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses and between said anodic pulses and succeeding cathodic pulses.

5. The method of claim 1 wherein said cathodic pulses and said anodic pulses succeed each other without intervening intervals of no electric current flow.

[illegible]

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**FIGURE: Sequential electrodeposition of metals using modulated electric fields for manufacture of circuit boards having features of different sizes**

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electroplating apparatus and plated in two steps according to the invention. The plating bath had the following composition: 60–65 g/L of copper sulfate, 166 g/L of sulfuric acid, about 50 parts per million (ppm) of cadmate ion, and about 300 ppm of polyethylene glycol (PEG).

In the first step of the plating process the pulsed reversing electric current had the following characteristics:

cathodic duty cycle, 33%; anodic duty cycle, 67%; average cathodic current density, 25 amperes per square foot (ASF), frequency of pulse train, about 333 Hz, and cathodic/anodic charge ratio ( $Q_c/Q_a$ ), 2.5. The plating was conducted for a period of 3 hours in the first step.

The second step of the plating process was then conducted by merely changing the waveform of the plating current. The bath was not changed, the board was not removed from the plating apparatus and no other processing steps were conducted.

In the second step of the plating process the pulsed reversing electric current had the following characteristics: cathodic duty cycle, 50%; anodic duty cycle, 10%; average cathodic current density, 25 amperes per square foot (ASF); cathodic current density, 12 ASF; anodic current density, 2 ASF; frequency of pulse train, about 100 Hz; and cathodic/anodic charge ratio ( $Q_c/Q_a$ ) 10. The plating was conducted for a period of 1 hour in the second step.

The results achieved are illustrated in FIGS. 4-6, FIG. 4 is a photomicrograph of a cross-section of the plated substrate showing the surface of the plated substrate with defects in the brass test panel are also visible.) FIGS. 5 and 6 are photomicrographs showing cross sections of the substrate at each end of the through hole showing a generally uniform plating of the surface of the substrate and the inner surface of the through-hole, with minimum excessive plating ("dog-ear") at the edge of the hole.

The invention having now been fully described, it should be understood that it may be embodied in other specific forms or variations without departing from its spirit or essential characteristics. Accordingly, the embodiments described above are to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing descriptions, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

1. A method for depositing a continuous layer of a metal onto a substrate having both hydrodynamically inaccessible recesses and hydrodynamically accessible recesses on its surface comprising

immersing as an electrode an electrically conductive substrate having a generally smooth surface being both at least one hydrodynamically inaccessible recess and at least one hydrodynamically accessible recess in said surface in an electrolyte bath containing ions of a metal to be deposited onto said surface.

immersing a counter electrode in said plating bath, in a first electroplating step, passing a first modulated reversing electric current between said electrodes, wherein

said first modulated reversing electric current comprises first cathodic pulses and first anodic pulses, said first cathodic pulses have a duty cycle less than about 50% and said first anodic pulses have a duty cycle greater than about 50%.

the charge transfer ratio of said first cathodic pulses to said first anodic pulses is greater than one, and the frequency of said first pulses ranges from about 10 Hertz to about 12000 Hertz; and

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in a second electroplating step, passing a second modulated reversing electric current between said electrodes, wherein said second modulated reversing electric current comprises second cathodic pulses and second anodic pulses.

said second cathodic pulses have a duty cycle greater than about 50% and said second anodic pulses have a duty cycle less than about 50%, the charge transfer ratio of said second cathodic pulses to said second anodic pulses is greater than one, and the frequency of said second pulses ranges from about 10 Hertz to about 5000 Hertz.

2. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses in said first and second electrolyzing steps.

3. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses in said first and second electroplating steps.

4. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses and between said anodic pulses and succeeding cathodic pulses in said first and second electrojecting steps.

5. The method of claim 1 wherein, in said first electroplating step, said cathodic pulses and said anodic pulses succeed each other without intervening intervals of no electric current flow.

6. The method of claim 1 wherein, in said first electrostimulating step, said cathodic pulses and said anodic pulses form a pulse train having a frequency between about 50 Hz and about 10000 Hertz.

7. The method of claim 1 wherein, in said first electro-  
plating step, said cathodic pulses and said anodic pulses  
form a pulse train having a frequency between about 100  
hertz and about 6000 Hertz.

8. The method of claim 1 wherein, in said first electro-sensing step, said cathodic pulses and said anodic pulses comprise a pulse train having a frequency between about 500 hertz and about 4000 Hertz.

9. The method of claim 1 wherein, in said first electroplating step, said cathodic pulses have a duty cycle of from about 30% to about 100%.

10. The method of claim 1 wherein, in said first electroplating step, said cathodic pulses have a duty cycle of from about 30% to about 15%.

11. The method of claim 1 wherein, in said first electro-  
plating step, said cathodic pulses have a duty cycle of from  
about 30% to about 30%.

12. The method of claim 1 wherein, in said first electro-  
lating step, said anodic pulses have a duty cycle of from  
about 50% to about 90%.

13. The method of claim 1 wherein, in said first electro-  
lating step, said anodic pulses have a duty cycle of from  
about 60-90 to about 99%.

14. The method of claim 1 wherein, in said first electro-  
plating step, said anodic pulses have a duty cycle of from  
about 70% to about 85%.

15. The method of claim 1 wherein said metal is selected from the group consisting of copper, nickel, cobalt, iron, and steel; said vacuum furnace has a duty cycle of less than about 70% to about 80%.

from the group consisting of copper, silver, gold, zinc, aluminum, nickel, tin, lead, bronze, brass, solder, and alloys thereof.

16. The method of claim 1 wherein, in said first electroplating step, a layer of metal of substantially uniform thickness is deposited on said surface and within said

17. The method of claim 1 wherein, in said first electro-  
lysis even the thickness of the metal layer decreased

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DOCUMENT-IDENTIFIER: US 6210555 B1  
TITLE: Electrodeposition of metals in small recesses for manufacture of high density interconnects using reverse pulse plating

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## US 6,210,555 B1

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immersing an electrically conductive substrate having a generally smooth surface having at least one small recess therein, wherein at least one transverse dimension of said recess is from about 5 micrometers to about 250 micrometers, in an electrolytic bath containing ions of a metal to be deposited onto said surface, immersing a counter electrode in said plating bath, passing an electric current between said substrate and said counter electrode.

said electric current is a modulated reversing electric current comprising a train of pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate, said cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%.

the charge transfer ratio of said cathodic pulses to said anodic pulses is greater than one, and the frequency of said pulse train ranges from about 10 Hertz to about 5000 Hertz.

2. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses.
3. The method of claim 1 wherein an interval of no

4. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses.

5. The method of claim 1 wherein said cathodic pulses and said anodic pulses succeed each other without intervening anodic pulses and succeeding cathodic pulses.

6. The method of claim 1 wherein said cathodic pulses and said anodic pulses form a pulse train having a frequency between about 50 Hertz and about 5000 Hertz.

7. The method of claim 1 wherein said cathodic pulses and said anodic pulses form a pulse train having a frequency between about 100 Hertz and about 3000 Hertz.

9. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 30% to about 1%.

10. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 30% to about 15%.

11. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 10% to about 20%.

12. The method of claim 1 wherein said anodic pulses have a duty cycle of from about 60% to about 99%.

14. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 70% to about 85%.

16. The method of claim 1 wherein a layer of metal of substantially uniform thickness is deposited on said surface

17. The method of claim 1 wherein the thickness of the metal layer deposited within said recesses is greater than the thickness of the metal layer deposited on said surface.

18. The method of claim 1 wherein said recesses are substantially filled with metal.

19. The method of claim 1 wherein at least one transverse dimension of said recess is from about 25 micrometers to

about 250 micrometers.

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20. The method of claim 1 wherein at least one transverse dimension of said recess is from about 50 micrometers to about 150 micrometers.

21. The method of claim 1 wherein amounts of conventional plating bath additives that are used in small amounts are minimized in said plating bath.

22. The method of claim 21 wherein said plating bath is

essentially devoid of said conventional plating bath additives that are used in small amounts.

24. The method of claim 1 wherein said plating is essentially devoid of additives that help to produce a level, uniform surface.

26. The method of claim 25 wherein amounts of conventional plating bath additives that are used in small amounts

27. The method of claim 25 wherein said plating bath is essentially devoid of said conventional plating bath additives that are used in small amounts.

28. The method of claim 27 wherein at least one of said  
 29. recesses is filled in a single plating step.

30. The method of claim 25 wherein said plating bath is essentially devoid of additives that help to produce a leveling of metal.

31. The method of claim 30 wherein at least one of said small recesses is filled in a single plating step.

32. The method of claim 25 wherein said plating bath contains conventional amounts of copper ions and a cyanide salt.

33. The method of claim 25 wherein said plating bath contains conventional anions of copper, zinc, sodium, acid, chloroide ions, and a conventional polyethylene glycol carrier compound.

ditional amounts of copper ions, sulfuric acid, chloride ions, and a conventional polyethylene glycol carrier compound.

34. The method of claim 33 wherein at least one of said small recesses is filled in a single plating step.

36. The method of claim 25 wherein said plating bath contains about 55 g/L of copper sulfate, about 9% by weight, amounts of copper ions, sulfuric acid, chloride ions, and a conventional polyethylene glycol carrier compound.

of sulfuric acid, about 50 parts per million of chloride ions and about 5% by weight of a conventional polyethylene glycol carrier compound.

electrically conducting substrate with a void-free deposit of metal comprising

generally smooth surface having at least one small recess therein, wherein at least one transverse dimension of said recess is from about 5 micrometers to about 250 micrometers, in an electroplating bath containing

ions of a metal to be deposited onto said surface, immersing a counter electrode in said plating bath, passing an electric current essentially continuously between said substrate and said counter electrode for a

period of time until said recess has been filled with said metal,



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